AMENDMENT TO THE CLAIMS

1. (Canceled).

2. (Currently Amended) ~~The process of claim 1, further including steps of:~~A process of implementing a logic circuit for logical operations based on a function

$$f_N = x_1 \text{ OR } (x_2 \text{ AND } (x_3 \text{ OR } (x_4 \text{ AND } \ldots x_N \ldots)))$$

or

$$f'_N = x_1 \text{ AND } (x_2 \text{ OR } (x_3 \text{ AND } (x_4 \text{ OR } \ldots x_N \ldots))),$$

comprising steps of:

a) selecting N as the number of variables of the logic circuit;

~~e~~b) defining a top portion of the logic circuit based on a pre-selected pattern of first and second gate types, the top portion defining at least a top level of the logic circuit and having N inputs and]N/3[outputs;~~,~~

~~d~~c) defining a ~~second~~ lower portion of the logic circuit having the same number of inputs as the number of outputs of the top portion;~~, and~~

~~e~~d) defining the inputs of the ~~second logic circuit~~lower portion as coupled to the outputs of the top portion; and

e) implementing the logic circuit as the defined top and lower portions with two-input gates to a depth between 2n and 2n+2 where n is an integer that N is between 3^n and 3^{n+1}.

3. (Currently Amended) ~~The process of claim 1, further including steps of:~~A process of implementing a logic circuit for logical operations based on a function

$$f_N = x_1 \text{ OR } (x_2 \text{ AND } (x_3 \text{ OR } (x_4 \text{ AND } \ldots x_N \ldots)))$$

or

$$f'_N = x_1 \text{ AND } (x_2 \text{ OR } (x_3 \text{ AND } (x_4 \text{ OR } \ldots x_N \ldots)))\text{,}$$

comprising steps of:

a) selecting N as the number of variables of the logic circuit;

~~b~~e) transforming groups of three variables of the function into new groups having at most two variables each;~~,~~

c~~d~~) replacing each new group with a single new variable;~~,~~

~~e~~d) defining a portion of the logic circuit in two-input gates of first and second gate types based on the new variables, the portion having a depth of no more than two levels of the logic circuit;~~,~~ and

~~f~~e) iteratively repeating steps (~~e~~b) to (~~e~~d) until there are no more than four variables; and

f) implementing the logic circuit in two-input gates having a depth between 2n and 2n+2 where n is an integer that N is between 3^n and 3^{n+1}.

4. (Original) The process of claim 3, wherein the portion defined during a first iteration defines a top level of the circuit having N inputs and]N/3[outputs, and each portion defined during successive iterations has the same number of inputs as the number of outputs of the portion defined during the next prior iteration and one-third (rounded up to the nearest integer) that number of outputs.

5. (Currently Amended) The process of claim 3, ~~further including selecting a bottom~~wherein the second portion of the logic circuit is based on the number of variables remaining when there are not more than four variables.

6. (Currently Amended) The process of claim 3, further including steps of:

~~e~~g) designing the logic circuit with N′ inputs, where N′ equals 3^n or $2*3^n$,

~~d~~h) setting odd-positioned inputs to a first binary value and even-positioned inputs to a second binary value in the N′-N most significant inputs, and

~~e~~i) removing gates that do not contribute to the function.

7. (Currently Amended) ~~The process of claim 1, further including steps of:~~A process of implementing a logic circuit for logical operations based on a function

$$f_N = x_1 \text{ OR } (x_2 \text{ AND } (x_3 \text{ OR } (x_4 \text{ AND } \ldots x_N \ldots)))$$

or

$$f'_N = x_1 \text{ AND } (x_2 \text{ OR } (x_3 \text{ AND } (x_4 \text{ OR } \ldots x_N \ldots))),$$

comprising steps of:

a) selecting N as the number of variables ~~to~~of the logic circuit;

b~~e~~) ~~for a predetermined value of N,~~ designing a first logic circuit having N-1 inputs and a pre-selected pattern of first and second gate types, the first logic circuit having a portion receiving I-1 most-significant input where I is smaller than N-1;~~, and~~

~~d~~c) substituting a predetermined logic circuit having I inputs for the portion of the first logic circuit; and

d) implementing the logic circuit with two-input gates to a depth between 2n and 2n+2 where n is an integer that N is between 3^n and 3^{n+1}.

8. (Original) The process of claim 7, wherein portions of the logic circuit are defined iteratively, the portion defined during a first iteration being a top level having N-1 inputs and](N-1)/3[outputs, and each portion defined during subsequent iterations having the same number of inputs as the number of outputs of the portion defined during the next prior iteration and one-third that number of outputs.

9. (Original) The process of claim 8, further including selecting a bottom portion based on the number of variables remaining when there are no more than four variables.

10. (Original) The process of claim 7, wherein the depth of the circuit is

$2n$, if $3^n < N \leq 3^n+3^{n-2}+3^{n-4}+\ldots$,

$2n+1$, if $3^n+3^{n-2}+3^{n-4}+\ldots < N \leq 2*3^n+3^{n-2}+3^{n-4}+\ldots$,

$2n+2$, if $2*3^n+3^{n-2}+3^{n-4}+\ldots < N \leq 3^{n+1}$.

11. (Currently Amended) ~~The process of claim 1, further including steps of:~~A process of implementing a logic circuit for logical operations based on a function

$$f_N = x_1 \text{ OR } (x_2 \text{ AND } (x_3 \text{ OR } (x_4 \text{ AND } \ldots x_N\ldots)))$$

or

$$f'_N = x_1 \text{ AND } (x_2 \text{ OR } (x_3 \text{ AND } (x_4 \text{ OR } \ldots x_N\ldots))),$$

comprising steps of:

a) selecting N as the number of variables of the logic circuit;

~~e~~b) designing the logic circuit with N′ inputs, where N′ > N and is 3^n or $2*3^n$, where n is an integer;

~~d~~c) setting odd-positioned inputs to a first binary value and even-positioned inputs to a second binary

value in the N'-N most significant inputs;~~, and~~

ed) removing gates that do not contribute to the function; and

e) implementing the logic circuit with two-input gates to a depth between 2n and 2n+2.

12. (Currently Amended) A logic circuit for performing logical operations designed by the process of claim ~~1~~7.

13 - 20. (Canceled).

21. (Currently Amended) The process of claim 3, further including, before step ~~d~~c),

moving a variable from each group of three variables to the new group.

22. (Canceled).

23. (New) A logic circuit for performing logical operations designed by the process of claim 2.

24. (New) A logic circuit for performing logical operations designed by the process of claim 3.

25. (New) The process of claim 3, wherein the depth of the circuit is

$2n$, if $3^n < N \leq 2*3^n$,

$2n+1$, if $2*3^n < N \leq 3^{n+1}$.